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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,133	12/10/2003	Chin-Te Kuo	4392-0147P	4685

2292 7590 03/06/2007

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EXAMINER	
SULLIVAN, CALEEN O	
ART UNIT	PAPER NUMBER
1756	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	03/06/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/731,133	KUO ET AL.	
	Examiner	Art Unit	
	Caleen O. Sullivan	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

Applicant's argument, see Reply to Office Action of October 16, 2006, filed 01/16/2007, with respect to Declaration have been fully considered and are persuasive. The objection has been withdrawn and Examiner accepts the Declaration filed with the application.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wiltshire ('401) in view of Figura ('109).

Wiltshire ('401) discloses the deposition of a photoresist layer over a horizontal surface of an initial film layer of a substrate in which an opening is created by etching of the photoresist layer. The first opening includes a horizontal surface and a vertical surface having width and height

dimensions. (See, para 0027). Examiner considers this the equivalent of providing a substrate with an opening exposing a sidewall and opening base surface as stated in claim 1.

Wiltshire ('401) also discloses a second film layer being deposited over the horizontal surface of the initial film layer of the substrate as well as the horizontal and vertical surfaces of the first opening, which is etched from the horizontal surface of the first opening such that the first opening has the same height dimension but has a smaller width dimension. (See, para 0027-0028). Examiner considers this the equivalent of forming a mask layer exposing a sidewall and portion of the opening base surface as stated in claim 1.

Wiltshire ('401) also discloses that a third film layer placed on the horizontal surface of the initial film layer and the horizontal and vertical surfaces of the first opening, this film layer including a dielectric. (See, para 0028). Examiner considers this to be the equivalent of forming a dielectric layer on the exposed sidewall and opening base surface as stated in claim 1.

Wiltshire ('401) goes on to disclose that once etching of the second film layer is complete this second film layer, which is a photoresist, is removed. (See, para 0028). Examiner considers this to be the equivalent of stripping the mask layer as stated in claim 9.

Wiltshire ('401) further discloses that a conductive material is deposited over horizontal surface of substrate and fills the opening. (See, para 0029). Examiner considers this to be the equivalent of forming a conductive layer over the substrate after the mask layer is stripped as stated in claim 10.

However, Wiltshire ('401) fails to disclose the formation of a mask layer that is tilted in an opening of a substrate that includes an exposed sidewall and base surface.

Figura ('109) does disclose a sloped masking layer, which is a layer of photoresist. This masking layer tapers from top to bottom within an opening on a substrate. (See col. 2, 4-7; 10-17). Examiner considers this to be the equivalent of a tilted mask layer as stated in claim 1.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant, to modify the teachings disclosed in Wiltshire ('401) with the masking layer which tapers from top to bottom as disclosed by Figura ('109) in order to achieve a substrate with an containing a tilted mask layer with a sidewall and opening base surface being exposed, because one achieves an opening that is smaller; therefore, going beyond the current capabilities of conventional photolithography processes to achieve a smaller feature size to increase the functional area of the substrate.

4. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wiltshire ('401) in view of Figura ('109) as applied to claims 1 and 9-10 above, and further in view of Lammert ('446) and Hu ('802).

Wiltshire ('401) and Figura ('109) are relied upon as discussed in the rejection of Claims 1 and 9-10 under 35 USC 103(a) set forth above in paragraph 5. Wiltshire ('401) and Figura ('109) fail to disclose heating a photoresist in order to reflow the photoresist into a desired profile.

Lammert ('446) discloses heating a photoresist within a temperature range and for a period of time to achieve a desired photoresist profile. Lammert ('446) also discloses that higher temperatures and longer bake times will produce more flow of the photoresist. In one embodiment of the inventive method described in Lammert ('446), the photoresist was heated between the temperature range of 150°C- 200°C and then flowed into the desired shape. (See col.4, 4-16). Examiner considers this to be the equivalent of heating the photoresist during reflow, as stated in

claim 3, within a temperature range of 100°C-150°C and a time range of 100-150 seconds as stated in claim 4.

However, Lammert ('446) fails to disclose a step of hardening the reflowed photoresist by post UV exposure to maintain the desired profile once it is obtained.

Hu ('802) also discloses the use of high temperature flow in order to reduce the size of a resist image of a feature with the added step of stabilizing the reflowed image by deep UV exposure. This freezes the resist profile at the desired reduced size. (See col.2, 23-28; 34-41). Examiner considers this to be the equivalent of hardening the photoresist layer by UV after reflow as stated in claim 5.

However, Lammert ('446) and Hu ('802) fail to disclose the limitation where the substrate is tilted in order to reflow the photoresist to form a tilted mask layer. It is inherent that the substrate would need to be tilted or rotated in order to reflow the photoresist material into the desired sloped or tilted formation as stated in claim 2.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant, to modify the teachings of Wiltshire ('401) and Figura ('109) with the step of heating a photoresist material at a temperature and for a period of time particular to the photoresist material in order to reflow the material into a desired shape and the step of deep UV exposure, as disclosed in Lammert ("446) and Hu ('802), because one would be able to achieve a particular profile of the photoresist material, and maintain the desired profile of the photoresist. Moreover, the step of tilting the substrate to reflow the photoresist material into the desired shape can be reasonably inferred as a necessity to achieve a tilted or sloped profile.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wiltshire ('401) and Figura ('109) as applied to claims 1 and 9-10 above, and further in view of Koizumi ('708).

Wiltshire ('401) and Figura ('109) are relied upon as discussed in the rejection of Claim 1 and 9-10 under 35 USC 103(a) set forth above in paragraph 5. Wiltshire ('401) and Figura ('109) fail to disclose an ozone ashing method for the removal of photoresist material.

Koizumi ('708) discloses that a photoresist is an organic substance and can be removed by ozone ashing. In this method a photoresist film is exposed to a hot gas, which contains ozone in order to remove the resist film by thermal decomposition. (See col.1, 14-19). Examiner considers this to be the equivalent of the ozone ashing step, which occurs before a dielectric layer is formed as stated in claim 6.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the teachings of Wiltshire ('401) and Figura ('109) with the ozone ashing method disclosed in Koizumi ('708) in order to remove the photoresist because very little damage occurs to the substrate during exposure to the ashing atmosphere.

6. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wiltshire ('401) and Figura ('109) as applied to claims 1 and 9-10 above, and further in view of Lin ('786).

Wiltshire ('401) and Figura ('109) are relied upon as discussed in the rejection of Claims 1 and 9-10 under 35 USC 103(a) set forth above in paragraph 5. Wiltshire ('401) and Figura ('109) fail to disclose the formation of an oxide layer in an opening in a substrate by liquid phase deposition, where the oxide layer formed is a dielectric.

Lin ('786) discloses a method where an oxide layer is formed in a trench within a substrate by liquid phase deposition, and the dielectric material is oxide. (See, claims 1, 6 and 8). Examiner considers this to be the equivalent of growing an oxide layer on an exposed sidewall and base surface of an opening within a substrate before a dielectric layer is formed, where the dielectric layer is the oxide layer formed by liquid phase deposition as stated in claims 7 and 8.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the teachings of Wiltshire ('401) and Figura ('109) with teachings of Lin ('786) in order to form a dielectric layer on the sidewall and base surface of a substrate by growing an oxide layer which is a dielectric on the sidewall and base surface of the substrate by liquid phase deposition, because the oxide layer formed by liquid phase deposition is selective for photoresist; therefore, it will not grow on the masking layer but instead only the sidewall of the trench in the substrate.

7. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wiltshire ('401) in view of Figura ('109) and Lammert ('446) and Hu ('802).

Wiltshire ('401) Figura ('109) Lammert ('446) and Hu ('802) are relied upon as discussed in the rejections of Claims 1-5 and 9-10 under 35 USC 103(a) set forth above in paragraphs 5 and 6.

Wiltshire ('401) also discloses the method described is applicable to semiconductor wafer as the substrate. (See, para 0027). It is also well known in the art that storage nodes are common components of a semiconductor, which typically has a pad dielectric layer thereon as stated in claim 11. Therefore, Wiltshire ('401) discloses coating a photoresist layer on the pad dielectric of the semiconductor substrate as stated in claim 11, when the initial film is deposited on the horizontal surface of the semiconductor wafer. (See, para 0027).

The disclosures in Figura ('109), Lammert ('446) and Hu ('802) are also related to constructing a semiconductor device, as are the limitations stated in claims 11-14. (See Figura: col. 4, 55; Lammert: col. 3, 19; Hu: col. 3, 5-9).

Lammert ('446) and Hu ('802) fail to disclose the limitation of claim 11 where the semiconductor substrate is tilted in order to reflow the photoresist to form a tilted mask layer. As stated above, in the rejection of claims 2-5 in paragraph 6, it is inherent that the semiconductor

substrate would need to be tilted in order to reflow the photoresist material into the desired sloped or tilted formation as stated in claim 11.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to combine the teachings of Wiltshire ('401) and Figura ('109) with Lammert ('446) and Hu ('802) because one could achieve a semiconductor device with a feature size that goes beyond the current capabilities of conventional photolithography processes in order to increase the functional area of the semiconductor device. This is accomplished by, achieving and then maintaining a desired profile of the photoresist within the semiconductor substrate by thermal reflow and then deep UV exposure, and then depositing the conducting layer within the opening after the photoresist is removed.

8. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wiltshire ('401) in view of Figura ('109) and Lammert ('446) and Hu ('802) as applied to claims 11-14 above, and further in view of Koizumi ('708).

Wiltshire ('401) Figura ('109) Lammert ('446) and Hu ('802) are relied upon as discussed in the rejection of Claims 1-5 and 9-10, in paragraphs 5 and 6, and as further discussed in the rejection of Claims 11-14 in paragraph 9, under 35 USC 103(a). Koizumi ('708) is relied upon as discussed in the rejection of Claim 6 under 35 USC 103(a), for its teachings of ozone ashing as set forth above in paragraph 7.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the teachings of Wiltshire ('401) and Figura ('109) and Lammert ('446) and Hu ('802) with the ozone ashing method disclosed in Koizumi ('708) in order to remove the photoresist material, because very little damage occurs to the semiconductor substrate during the exposure to the ashing atmosphere.

9. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wiltshire ('401) in view of Figura ('109) and Lammert ('446) and Hu ('802) as applied to claims 11-14 above, and further in view of Lin ('786).

Wiltshire ('401) Figura ('109) Lammert ('446) and Hu ('802) are relied upon as discussed in the rejection of Claims 1-5 and 9-10 in paragraph 5 and 6, and as further discussed in the rejection of Claims 11-14 in paragraph 9, under 35 USC 103(a). Lin ('786) is relied upon as discussed in the rejection of claims 7-8 under 35 USC 103(a) as set forth above in paragraph 8 for its teachings of forming an oxide layer by liquid phase deposition.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the teachings of Wiltshire ('401) and Figura ('109) and Lammert ('446) and Hu ('786) with teachings of Lin ('786) in order to form a dielectric layer on the sidewall and surface of a storage node of a semiconductor substrate by growing an oxide layer which is a dielectric on the sidewall and surface of the storage node by liquid phase deposition, because the oxide layer formed by liquid phase deposition is selective for photoresist; therefore, it will not grow on the masking layer but instead only the sidewall of the trench in the substrate.

10. Claims 1-4 and 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Flanders ('225) in view of Wiltshire ('401). Wiltshire ('401) is relied upon as discussed in the rejection of claims 1, 9-10 under 35 USC 103(a), in paragraph 3 above.

Flanders ('225) discloses a tapered ion implantation process to eliminate printable alternating phase shift features. The method consists of first forming at least one opaque image on a surface of a substrate, by forming a layer of opaque material on the substrate that is subsequently patterned by conventional lithography processes. (See, col.4, 7-42). Next a patterned resist layer is formed on the substrate and opaque images formed on the substrate where portions of the substrate and opaque

images are protected and the other portions remain exposed. (See, col.4, 43-58; claim1; Fig.2b). This meets the limitation of claim one where a substrate is provided having an opening that exposes a sidewall and an opening base surface. This first patterned resist layer is also subjected to a hardening process.

The next step in the process disclosed in Flanders ('225) is to form a second patterned resist layer, which is formed by a conventional deposition process and lithography. (See, col. 5, 1-7; Fig.2c). After this second patterned photoresist layer is formed the resist is subjected to a reflow process in which a sloped profile is formed at edges. This meets the limitation of claim 1 where a titled mask layer is formed and the limitations of claim 2. (See, col. 4,66-col.5, 16; claim 1; Fig.2c-2d). The reflow process disclosed in Flanders ('225) takes place in an oven or furnace at a temperature between 75°C-140°C, for 10-40 minutes, which meets the limitations of claims 3 and 4. This sloped profile is then transferred to the substrate and then the first and second resists are removed as recited in claim 9. (See, col.5, 25-30; col. 6, 50-54; claim 1). Although Flanders ('225) does not teach a step where the substrate is tilted to reflow the photoresist to form a tilted mask layer, it is inherent the substrate would need to be tilted or rotated in order to reflow the photoresist material into the desired sloped or tilted formation as stated in claim 2.

However, Flanders ('225) does fail to teach the limitation of claim 1, where a dielectric layer is formed on the exposed sidewall and base surface of the opening on the substrate. Moreover, Flanders ('225) fails to disclose the formation of a conductive layer over the substrate after the tilted mask layer is stripped as recited in claim 10. Wiltshire ('410) teaches such process steps.

As discussed in the rejection of claims 1 and 9-10 under 35 USC 103(a) in paragraph 3 above, Wiltshire ('401) teaches the formation of a masking layer within an opening on a substrate, where a sidewall and opening base surface are exposed. (See, para 0027-0028). Wiltshire ('401)

discloses that after the second resist layer is removed a third film layer, which includes a dielectric is placed on the horizontal surface of the initial film layer and the horizontal and vertical surfaces of the first and second opening. (See, para 0028). This disclosure meets the limitation of claim 1 where a dielectric layer is formed on the exposed sidewall and opening base surface.

Wiltshire ('401) also discloses that after etching of the second film layer, a photoresist layer, the film layer is removed, (See, para 0028) and a conductive material layer is deposited over the horizontal surface of the substrate and fills the first and second openings (See, para 0029). This disclosure meets the limitation of claim 10, where a conductive layer is formed over the substrate after the mask layer is stripped.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the teachings of Flanders ('225) in view of the teachings of Wiltshire ('401), because Wiltshire teaches that one can form a dielectric layer and a conductive layer on a substrate such as the one disclosed in Flanders ('225). Moreover, the step of tilting the substrate to reflow the photoresist material into the desired shape can be reasonably inferred as a necessity to achieve a tilted or sloped profile.

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Flanders ('225) in view of Wiltshire ('401) as applied to claims 1-4 and 9-10 in paragraph 10 above, and further in view of Hu ('802).

Flanders ('225) and Wiltshire ('401) fail to disclose a step of hardening the reflowed photoresist by post UV exposure to maintain the desired profile once it is obtained. However, Hu ('802) discloses such a process step.

Hu ('802) discloses the use of high temperature flow in order to reduce the size of a resist image of a feature with the added step of stabilizing the reflowed image by deep UV exposure. This

freezes the resist profile at the desired reduced size. (See col.2, lines 23-28 and lines 34-41). This disclosure meets the limitation of claim 5, where a photoresist layer is hardened by UV after reflow as stated in claim 5.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the combination of Flanders ('225) in view of Wiltshire ('401), with the teachings of Hu ('802) because Hu ('802) teaches one can maintain a sloped profile of the photoresist using the stabilization step of post reflow UV exposure.

12. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Flanders ('225) in view of Wiltshire ('401) as applied to claims 1-4 and 9-10 in paragraph 10 above, and further in view of Koizumi ('708).

Flanders ('225) in view of Wiltshire ('401) fails to disclose an ozone ashing method for the removal of photoresist material. However, Koizumi ('708) discloses such a process.

Koizumi ('708) discloses that a photoresist is an organic substance and can be removed by ozone ashing. In this method a photoresist film is exposed to a hot gas, which contains ozone in order to remove the resist film by thermal decomposition. (See col.1, 14-19). This disclosure meets the limitation of claim 6.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the combination of Flanders ('225) in view of Wiltshire ('401) with the ozone ashing method disclosed in Koizumi ('708) in order to remove the photoresist because very little damage occurs to the substrate during exposure to the ashing atmosphere.

13. Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Flanders ('225) in view of Wiltshire ('401) as applied to claims 1-4 and 9-10 in paragraph 10 above, and further in view of Lin ('786).

Flanders ('225) in view of Wiltshire ('401) fails to disclose the formation of an oxide layer in an opening on a substrate by liquid phase deposition, where the oxide layer formed is a dielectric. Lin ('786) discloses such process steps.

Lin ('786) discloses a method where an oxide layer is formed in a trench within a substrate by liquid phase deposition, and the dielectric material is oxide. (See, claims 1, 6 and 8). This disclosure meets the limitations of claims 7 and 8, where an oxide layer is grown on an exposed sidewall and base surface of an opening within a substrate before a dielectric layer is formed, where the dielectric layer is the oxide layer formed by liquid phase deposition.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the combination of Flanders ('225) in view of Wiltshire ('401) with the teachings of Lin ('786) in order to form a dielectric layer on the sidewall and base surface of a substrate by growing an oxide layer which is a dielectric on the sidewall and base surface of the substrate by liquid phase deposition, because the oxide layer formed by liquid phase deposition is selective for photoresist; therefore, it will not grow on the masking layer but instead only the sidewall of the trench in the substrate.

Response to Arguments

14. Applicant's note regarding the incorrect citation of the Wiltshire ('401) reference, on the PTO-892 form is noted. This information has been corrected in the PTO-892 that accompanies this rejection.

15. Applicant's arguments filed on 01/16/2007 have been fully considered but they are not persuasive.

16. Applicant argues the rejection of claim 1 is improper because Wiltshire ('401) teaches anisotropic etching along the horizontal surface of the initial film layer and the openings, which

means the second film layer covers all the sidewalls of the openings. Therefore, applicant argues Wiltshire ('401) does not teach a mask layer that covers a portion of a sidewall and base surface of an opening on a substrate, while a portion of the sidewall and other portion of the base surface are exposed.

Examiner finds that anisotropic etching is not a claimed embodiment of the invention; therefore, applicant's argument provides a limitation that is not germane to the claims as amended, and unduly limits the teachings of Wiltshire ('401). Moreover, Examiner finds the teachings of Wiltshire ('401) in paragraphs 0027-0028 disclose forming a mask layer, although not tilted, where a portion of the sidewall and base surface of the opening is covered and the other portion of the sidewall and base surface of the opening is exposed.

17. Applicant argues the rejection of claim 1 is improper because Figura ('109) teaches anisotropic etching to form a sloped masking layer, which means that while the underlying insulation layer is exposed all of the sidewalls of the opening are still covered by the sloped masking layer. Therefore, applicant argues Figura ('109) does not teach a tilted mask layer where a portion of the sidewall and base surface of the opening are covered while the other portion of the sidewall and base surface are exposed.

Examiner finds that anisotropic etching is not a claimed embodiment of the invention; therefore, applicant's argument provides a limitation that is not germane to the claims as amended, and unduly limits the teachings of Figura ('109). Moreover, Examiner finds that the teachings of Figura ('109) in Col.2, 2-17 discloses formation of a tilted mask layer where a portion of a sidewall and opening base surface are covered while the other portion of said sidewall and opening base surface are exposed.

18. Applicant also argues the rejection of claim 11 is improper because there is no teaching or suggestion in Lammert ('446) to form a single-sided conductor without using extra lithography process. However, Examiner finds that such a limitation is not stated in the claims; therefore, unduly limiting the teachings of Lammert ('446). Moreover, applicant claims are written using the open language comprising; therefore, allowing for the inclusion of extra lithography steps.

19. Applicant has not presented arguments in reference to Koizumi ('708) or Lin ('786).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Caleen O. Sullivan whose telephone number is 571-272-6569. The examiner can normally be reached Monday- Friday, 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Huff can be reached on 571-272-1385. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

COS
2/23/07

MARK F. HUFF
SUPERVISORY PATENT EXAMINER
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